

## Multistandard Sound IF

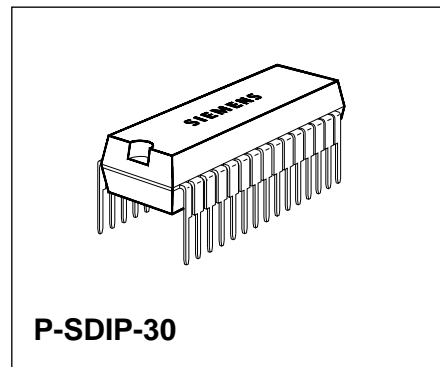
TDA 6160-2S

### Preliminary Data

Bipolar IC

#### Features

- Sound carrier mixer
- VCO
- Programmable Divider
- Reference divider with crystal oscillator
- Phase comparator
- Operational amplifier for PLL filter
- I<sup>2</sup>C bus interface
- 3 identical FM channels with limiter amplifiers and coincidence demodulators.



Type	Ordering Code	Package
TDA 6160-2S	Q67000-A5184	P-SDIP-30

#### Functional Description

Multistandard sound IF-device consisting of a mixer as a frequency converter, a voltage-controlled oscillator (VCO) that can be continuously tuned in 10-kHz increments with crystal accuracy by means of a PLL, and three following parallel FM-limiter amplifiers with coincidence demodulators.

The switching functions and setting of the PLL are controlled on an I<sup>2</sup>C bus.

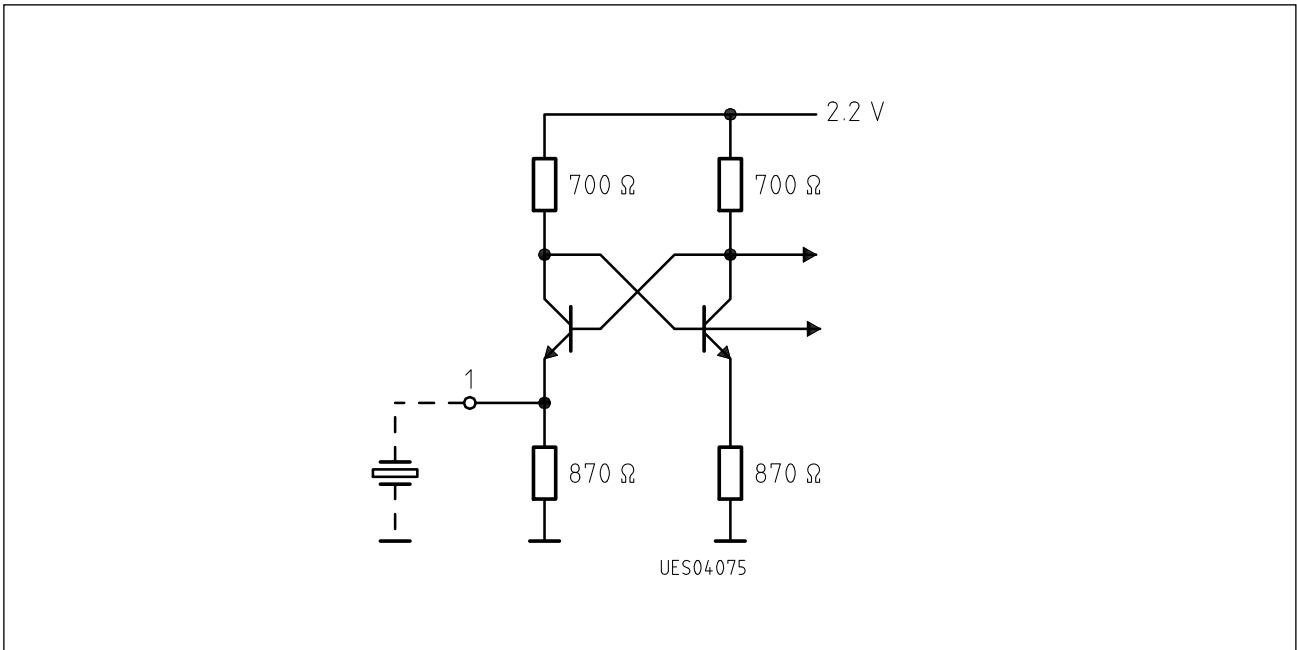
#### Application

For use in satellite receivers.

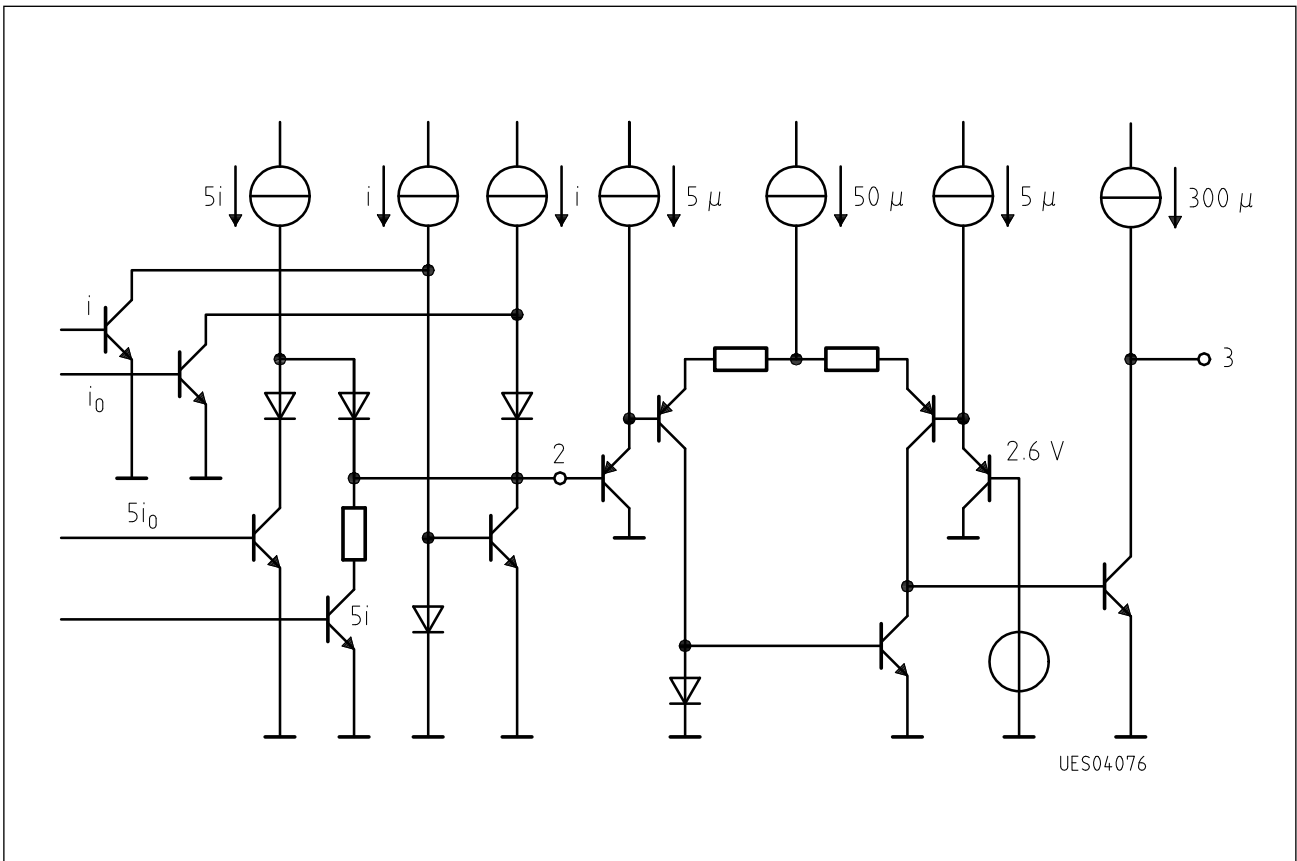
## Pin Functions

Pin No.	Function
1	Quartz oscillator
2	PD-output / integrator input ( $f_{REF}, f_{CY}$ )
3	Integrator output ( $V_D$ )
4	VCO
5	Chip address switching (CA)
6	Demodulator circuit (IF-1)
7	Demodulator circuit (IF-1)
8	AF-output 1
9	Demodulator circuit (IF-2)
10	Demodulator circuit (IF-2)
11	AF-output 2
12	Demodulator circuit (IF-3)
13	Demodulator circuit (IF-3)
14	AF-output 3
15	NC
16	NC
17	IF-input 3
18	$V_S$ (analog)
19	IF-input 2
20	Ground (analog)
21	IF-input 1
22	IF-reference
23	Mixer output 2
24	Mixer output 1
25	Mixer input (reference)
26	Mixer input
27	Ground (digital)
28	$V_S$ (digital)
29	I <sup>2</sup> C bus (SCL)
30	I <sup>2</sup> C bus (SDA)

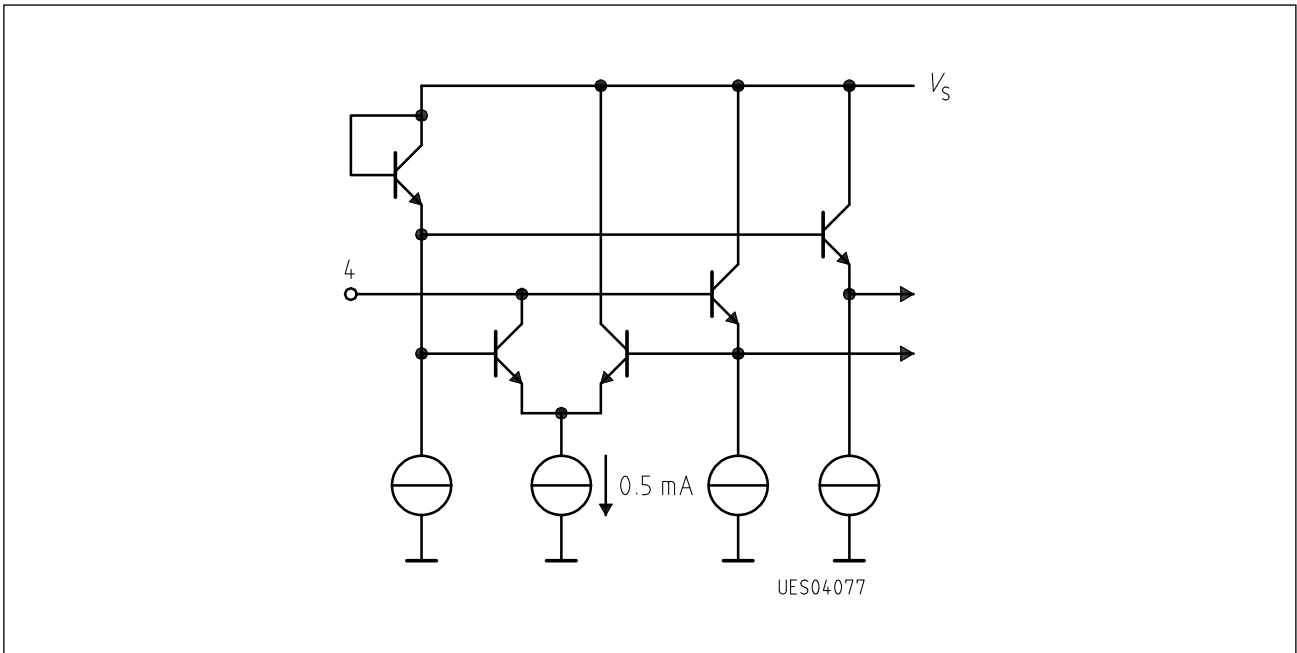
Pin Functions



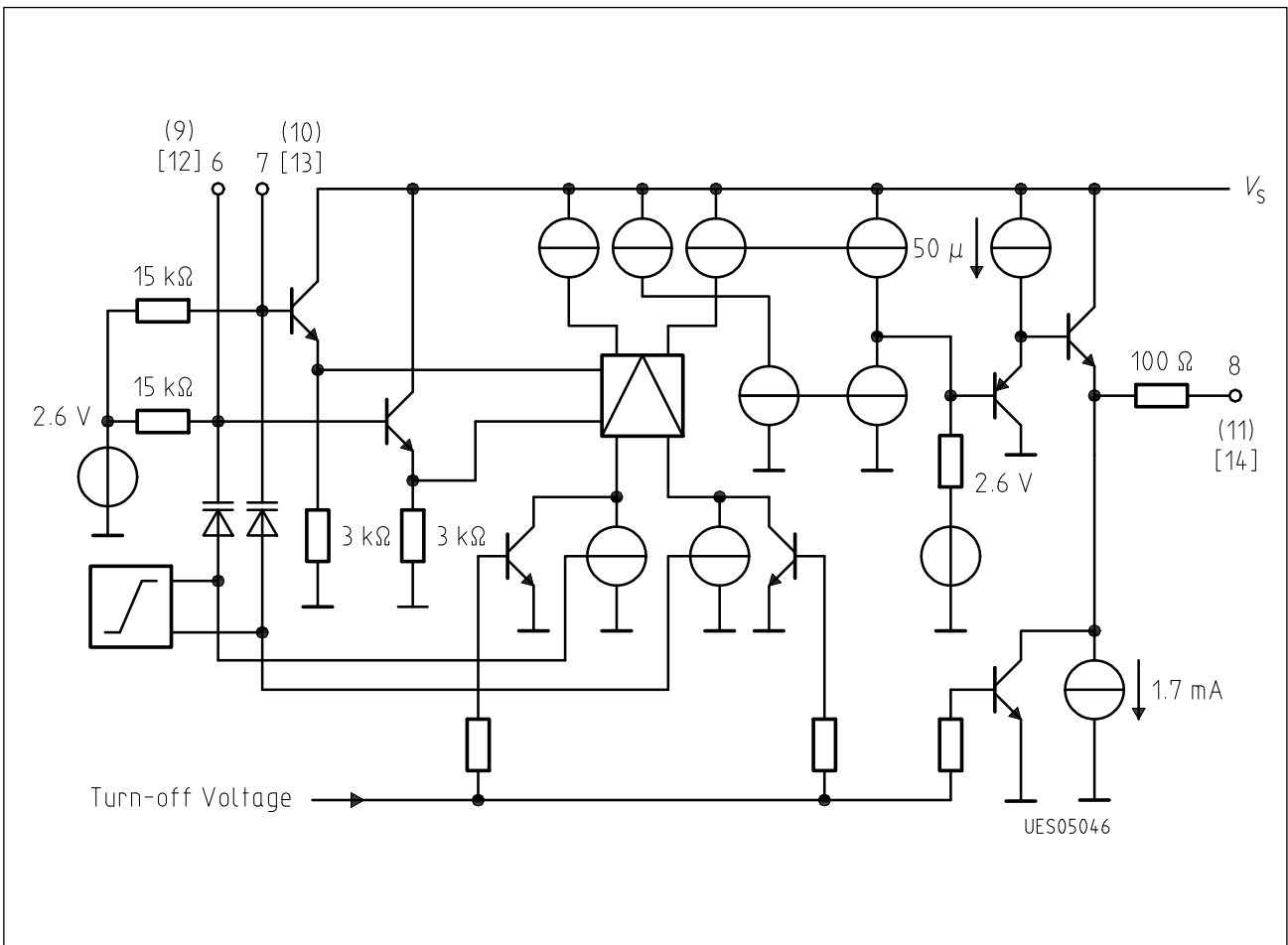
Pin 1



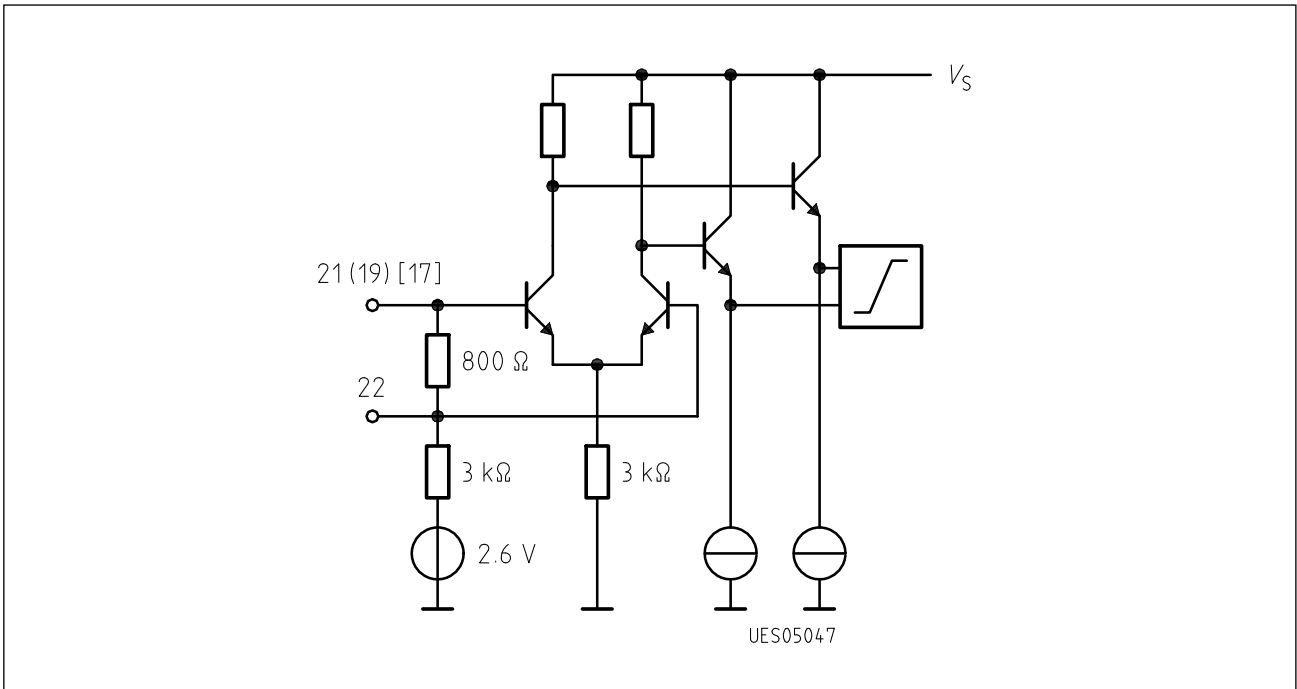
Pin 2/3



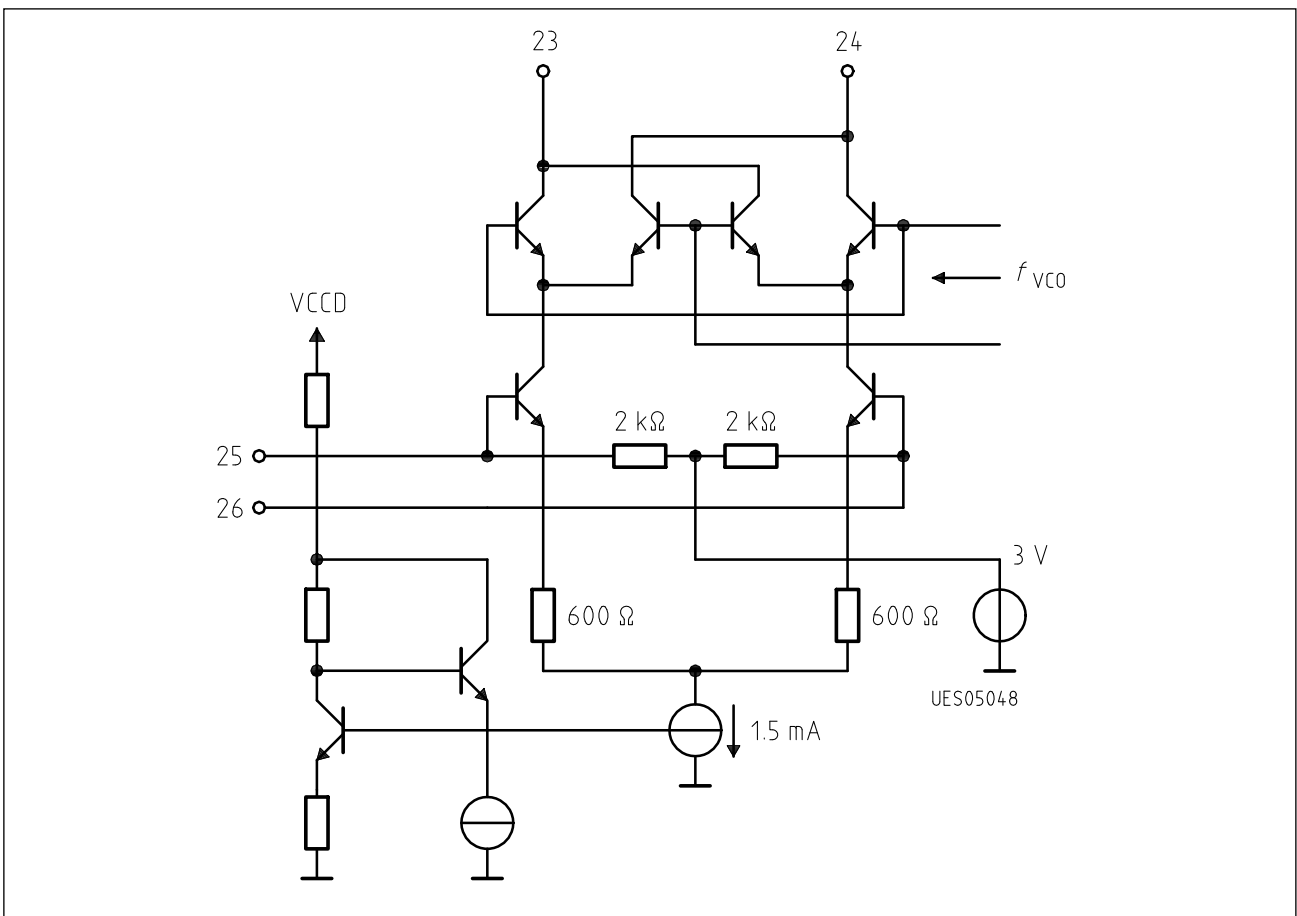
Pin 4



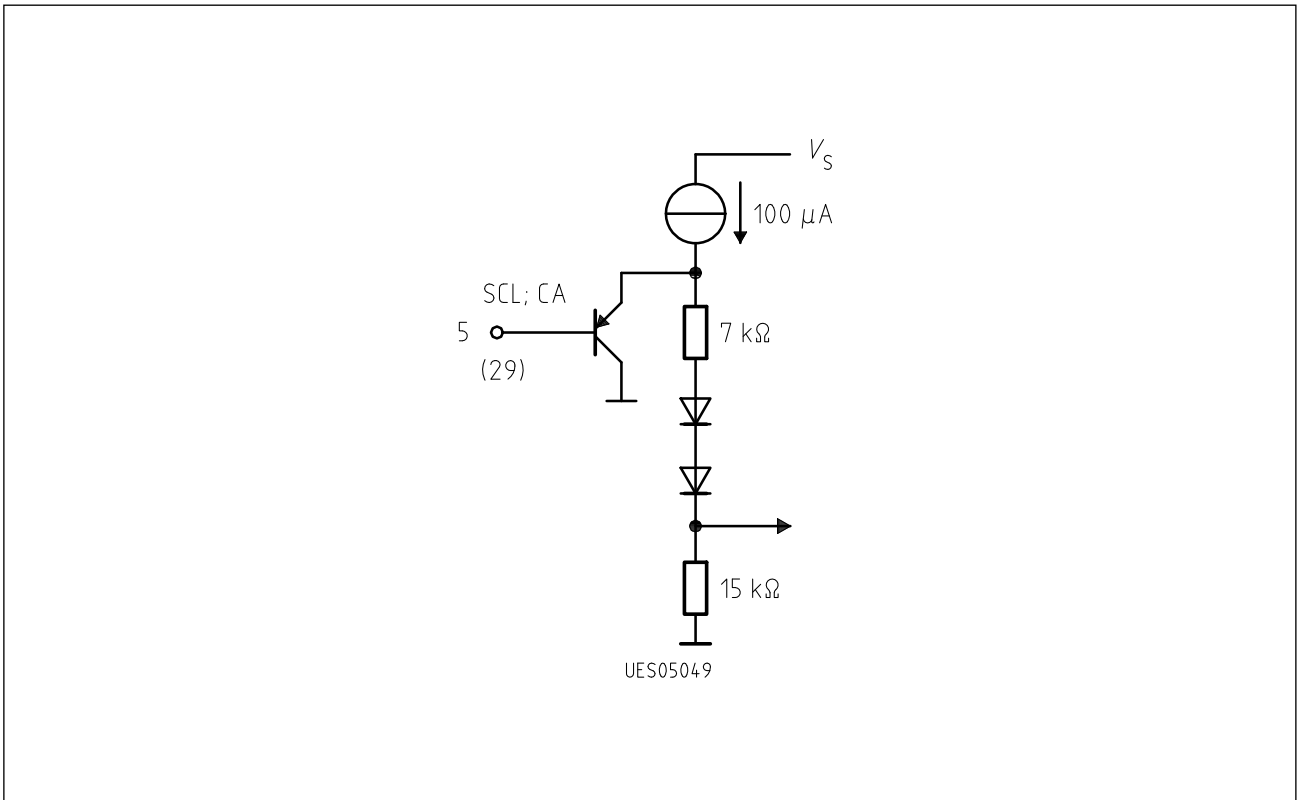
Pin 6/7/8; 9/10/11; 12/13/14



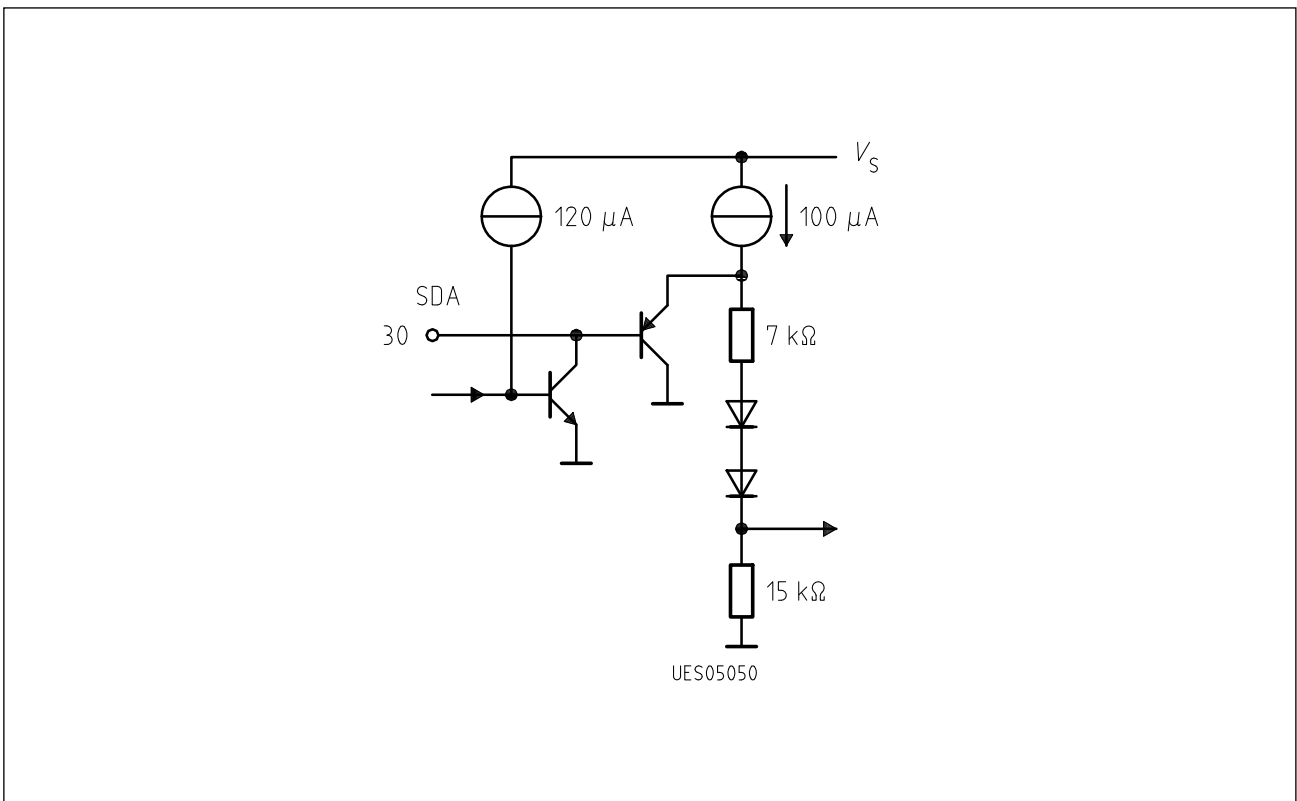
Pin 21; 19; 17/22



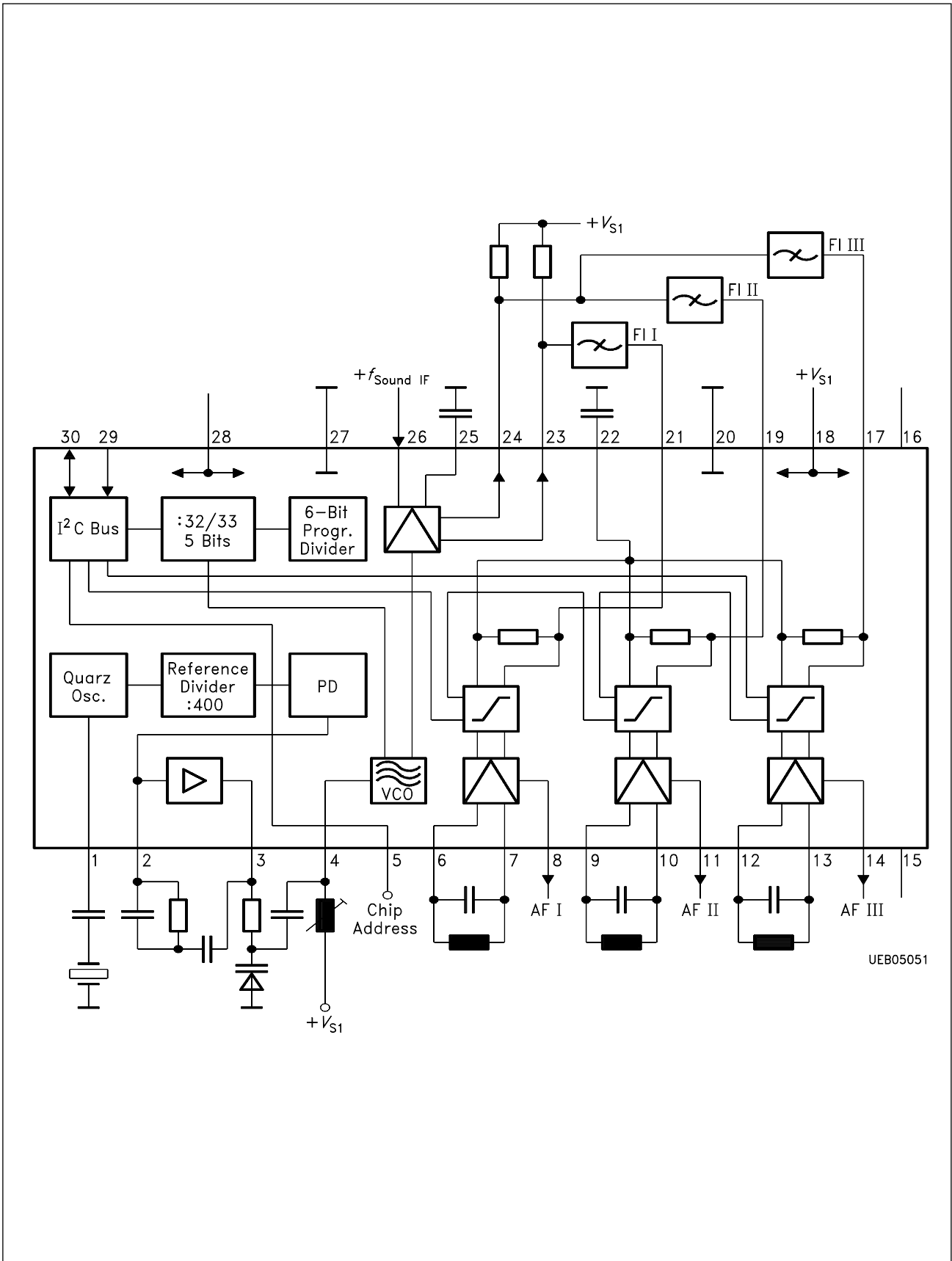
Pin 23/24/25/26



Pin 5; 29



Pin 30



UEB05051

Block Diagram

### Circuit Description

The sound intermediate frequencies contained in the baseband of a demodulated FM satellite signal can lie between 5 and 9 MHz. This band of frequencies is applied ready filtered to the input of the converter mixer. The purpose of this mixer is to convert the different sound IFs in the baseband to fixed output frequencies (eg 10.7/10.52 MHz). These frequencies are then fed by external filters to the inputs of the three sound IF-amplifiers.

The VCO of the mixer can be continuously tuned between 14.5 and 20 MHz in 10-kHz increments with crystal accuracy by means of a PLL-circuit.

The setting of the programmable divider and the cutting in and out of the sound IF-amplifiers are controlled on the I<sup>2</sup>C bus.

Pin 5 (CA) offers two switchable chip addresses to enable parallel operation of two devices.

All pins are guarded against electrostatic discharge. SCL and SDA include special protective structures to permit continued bus operation when the device is switched off.

### PLL

The VCO-signal, DC coupled internally, is applied to the PLL-input. It passes through a programmable divider ( $N = 1024$  to  $2047$ ) and is then compared to a reference frequency ( $f_{REF} = 10$  kHz) in a digital frequency/phase detector. This frequency is derived from a 4-MHz crystal oscillator whose signal is divided by 400.

The phase detector has a charge-pump push-pull current output. If the negative edge of the divided VCO-signal appears before the negative edge of the reference signal, the current source  $I+$  will pulse for the duration of the phase difference. In the reverse case it is the current sink  $I-$ . If both signals are in-phase, the output is high-impedance and the PLL is locked in. The current pulses are filtered by means of an integrator (internal operational amplifier with external RC-circuitry).

The pump current can be switched between the two values 1 and 5 by software with a control bit 5l. This permits a change in the control response during and after the lock-in state.

### I<sup>2</sup>C Bus Interface

Information is exchanged between the processor and the sound IF-device on an asynchronous bidirectional data bus. The timing for this comes from the processor (input SCL), while pin SDA-functions as an input or output depending on the direction of the data (open collector; external pull-up resistor).

The data from the processor go to an I<sup>2</sup>C bus controller and are filled in registers (latches 0 to 2) according to their function. When the bus is not busy, both lines are in marking state (SDA, SCL are high). Each telegram begins with the start condition: SDA goes low while SCL remains high. All further exchanges of information are while SCL is low and are read by the controller with the positive clock edge. If SDA goes high while the clock is high, the PLL recognizes this as a stop condition and thus the end of the telegram.

For what follows, refer to the table of logic assignments below.

All telegrams are transferred byte by byte, followed by a ninth clock pulse during which the controller pulls the SDA-line to low (i.e. acknowledge condition). The first byte consists of seven address bits with which the processor selects the PLL from among several peripheral devices (chip select). The



eighth bit is always low. The first bit of the first or third data byte in the data part of the telegram determines whether a divider ratio or control information will follow. In every case the first byte must be followed by a byte of the same data type (or a stop condition). When the supply voltage is applied, a power-on reset circuit prevents the PLL from pulling the SDA-line to low and thus blocking the bus.

**Logic Allocations**

Address byte	0	1	0	0	0	MA1	MA0	R/W	A	
Progr. divider byte 1	0	0	n10	n9	n8	n7	n6	n5	A	
Progr. divider byte 2	n4	n3	n2	n1	n0	0	0	0	A	
Control information	1	5I	Z2	Z1	Z0	T2	T1	T0	A	
Address byte 1	0	1	0	0	0	1	0	0	A	= H44
Address byte 2	0	1	0	0	0	1	1	0	A	= H46

Chip address (CA)  
 pin 5 on:                      ground            = address byte 1  
                                        $V_S$  or open    = address byte 2

**Test Mode**

T2, T1, T0 = 0, 0, 0	normal operation
T2, T1, T0 = 1, 0, 0	pin 2            = $f_{REF}$
T2, T1, T0 = 1, 1, 0	pin 2            = $f_{CY}$
T2, T1, T0 = 1, 1, 1	pin 2            = tristate
T2, T1, T0 = 0, 1, 1	pin 2            = high-impedance = pin 3 high-impedance

**IF-Muting Circuits**

Z2, Z1, Z0 = 0, 0, 0	normal operation	
Z2, Z1, Z0 = 0, 0, 1	IF 3	= off (output 14 high-impedance)
Z2, Z1, Z0 = 0, 1, 0	IF 2	= off (output 11 high-impedance)
Z2, Z1, Z0 = 0, 1, 1	IF 1 = on; IF 2/IF 3 = off	
Z2, Z1, Z0 = 1, 0, 0	IF 1	= off (output 8 high-impedance)
Z2, Z1, Z0 = 1, 0, 1	IF 1 = off; IF 2 = on; IF 3 = off	
Z2, Z1, Z0 = 1, 1, 0	IF 3 = on; IF 1/IF 2 = off	
Z2, Z1, Z0 = 1, 1, 1	IF 1, IF 2, IF 3 = off	

## Telegram Examples

Start-AB-DB1-DB2-CI-Stop	Start = start condition
	AB = address byte
Start-AB-CI-DB1-DB2-Stop	DB1 = divider byte 1
Start-AB-DB1-Stop	DB2 = divider byte 2
	CI = control information
Start-AB-CI-Stop	Stop = stop condition

## Converter Mixer + VCO

In the converter mixer the sound subcarriers (frequency band approx. 5 to 9 MHz) contained in the baseband of the received composite signal are converted to an output frequency of 10.52 MHz or 10.7 MHz for example. The two mixer outputs are designed as open-collector outputs.

The VCO has internal feedback and its frequency of 15.5 to 19.7 MHz is determined by an external resonant circuit with a varactor diode that is tuned by the PLL. The resonant circuit is connected to the supply voltage by its low side.

## IF-Limiter with Demodulators

The limiter amplifiers are implemented as balanced five-stage, capacitively coupled differential amplifiers. All there limiter inputs have a common reference (pin 22).

The output signals of the limiter amplifiers are fed direct and via an external phase-shifter circuit to the coincidence demodulators. The AF-signals can be brought out an disconnectible (by Z2, Z1, Z0) AF output stages. The outputs are high-impedance when they are disconnected.

## Absolute Maximum Ratings

$T_A = 0$  to  $70$  °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	$V_{18}, V_{28}$	0	6	V
AF-output	$I_8, I_{11}, I_{14}$	- 1.5	3	mA
AF-output	$V_8, V_{11}, V_{14}$		$V_{16}$	V
Demodulators	$V_{6/7}, V_{9/10}, V_{12/13}$	0	$V_{16}$	V
IF-inputs	$V_{17}, V_{19}, V_{21}$	0	$V_{16}$	V
Mixer outputs	$V_{23}, V_{24}$		7	V
VCO	$V_4$		7	V
Crystal oscillator	$V_1$	0	1.5	V
Junction temperature	$T_j$		150	°C
Storage temperature	$T_{stg}$	0	125	°C
Thermal resistance	$R_{th SA}$		65	K/W

All voltage values are referred to ground (pin 20, pin 27), unless stated otherwise.

All currents are designated according to the source and sink principle, i.e. if the device pin is to be regarded as a sink (the current flows into the stated pin to internal ground), it has a negative sign, and if it is a source (the current flows from  $V_S$  across the designated pin), it has a positive sign.

## Operating Range

Supply voltage	$V_{18}, V_{28}$	4.5	5.5	V
Input frequency range of converter mixer	$f_{i26}$	5	9	MHz
Input frequency range of sound IF-amplifiers (- 3 dB)	$f_{i17, 19, 21}$	5	15	MHz
VCO-frequency	$f_{O4}$	5	20	MHz
Ambient temperature	$T_A$	0	70	°C

## Characteristics

$V_S = 5\text{ V}$ ;  $T_A = 25\text{ °C}$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current drain (analog section)	$I_{18}$		33	42	mA	
Current drain (digital section)	$I_{28}$	20	35	44	mA	
Phase-detector charge current	$I_{PD}$	$\pm 32$ $\pm 160$	$\pm 40$ $\pm 250$	$\pm 75$ $\pm 360$	$\mu\text{A}$ $\mu\text{A}$	I 5I

## Mixer

### Static Characteristics

Mixer output currents	$I_{23, 24}$		1.1	3.5	mA	$V_{25} = V_{26}$
Output-current difference	$I_{23} - I_{24}$		100		$\mu\text{A}$	$V_{25} = V_{26}$
Mixer inputs	$V_{25, 26}$		3		V	

### Dynamic Characteristics

Input voltage for IMA > 60 dB	$V_{26}$		180	230	mVrms	SC1 = 6 MHz; SC2 = 6.5 MHz; SC3 = 7 MHz; $V_{SC1} = V_{SC2} = V_{SC3}$
Input-frequency band	$f_{I26}$	5		9	MHz	
Input-resistance	$R_{25/26}$		4		k $\Omega$	
Output-frequency band	$f_{O23/24}$		11		MHz	
Frequency band of VCO	$\Delta f_4$	15		20	MHz	
Mixer gain	$G_{Mi}$	- 8	- 4	- 2	dB	$R_L = 470\ \Omega$
Output-voltage range on mixer		$V_{18}$ - 0.4		$V_{18}$ max	V	IMA > 55 dB; $V_{25/26} < 180\text{ mVrms}$

## Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

## Sound IF (for all three amplifiers)

### Static and Dynamic Characteristics

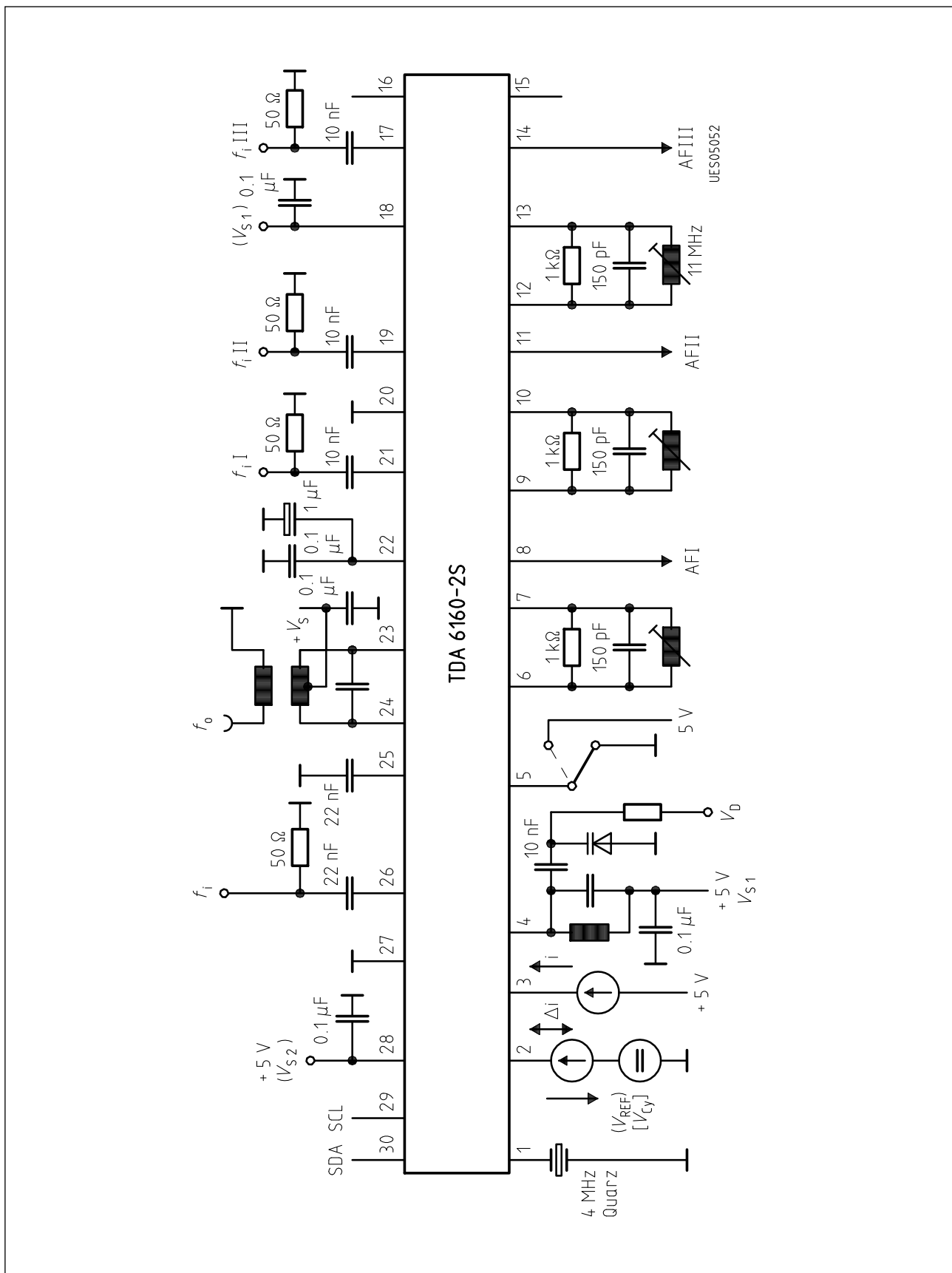
Input-frequency band	$f_{17, 19, 21}$	5		15	MHz	
Input voltage to activate limiting ( $V_{qAF} - 3$ dB)	$V_{17, 19, 21}$		70	250	$\mu$ V	$f_{117, 19, 21} = 10.7$ MHz; $\Delta f = 30$ kHz; $f_{mod} = 1$ kHz
AF-output voltage	$V_{8, 11, 14}$	150	220	300	mV	$f_{117, 19, 21} = 10.7$ MHz; $\Delta f = 30$ kHz; $V_{117, 19, 21} = 10$ mV, $f_{mod} = 1$ kHz
Distortion factor	$THD_{8, 11, 14}$			0.2	%	$f_{117, 19, 21} = 10.7$ MHz; $\Delta f = 30$ kHz; $V_{117, 19, 21} = 10$ mV, $f_{mod} = 1$ kHz
AM-rejection	$a_{AM}$		45		dB	$V_{117, 19, 21} = 20$ to 100 mV; $m = 30\%$
AM-rejection	$a_{AM}$		25		dB	$V_{117} = 2$ mV; $m = 30\%$
AF-output DC-voltage			2.2		V	

### Design Notes

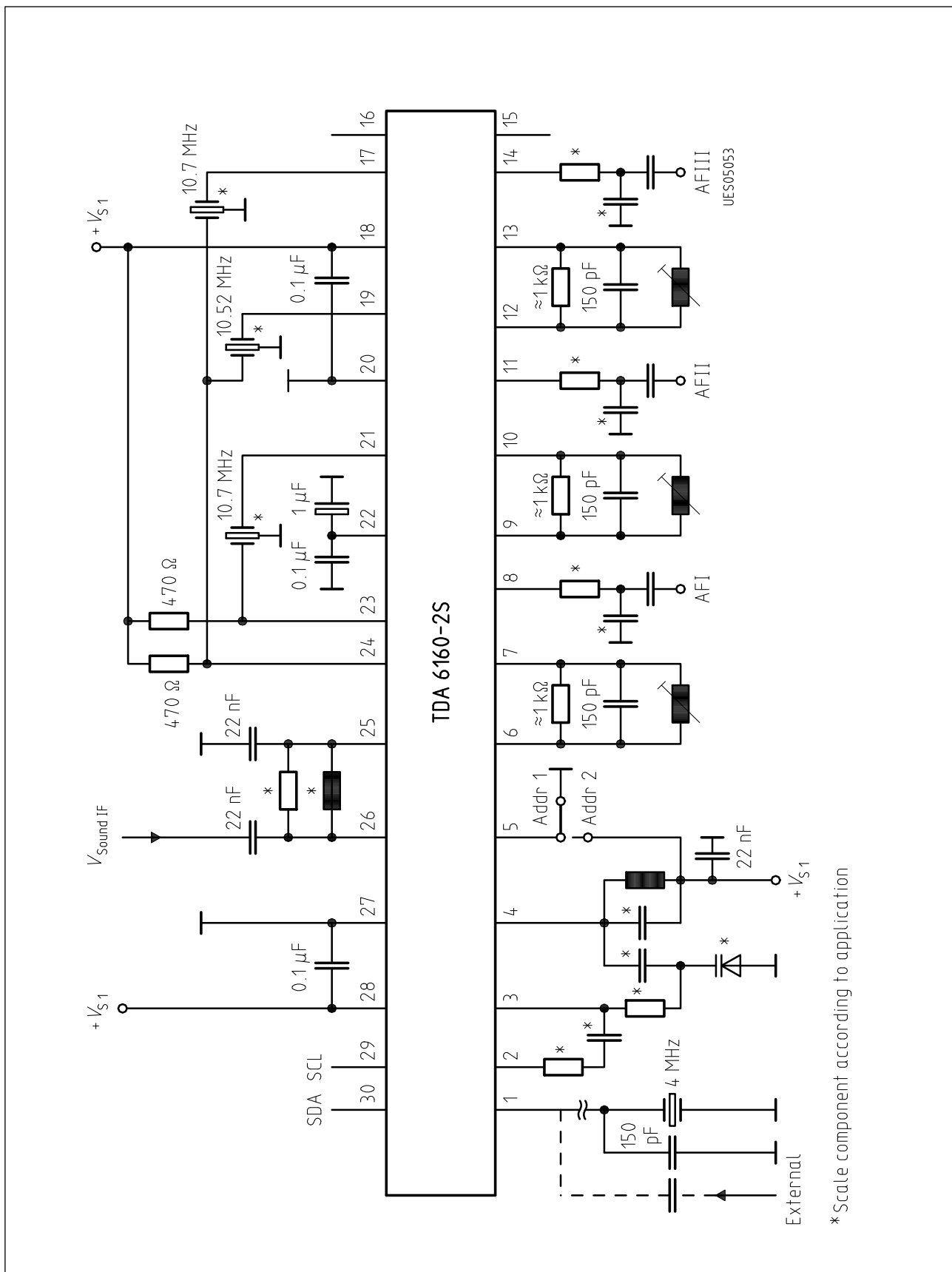
Sound IF-input resistance	$R_{17/22}$ $R_{19/22}$ $R_{21/22}$		800		$\Omega$	
Demodulator input resistance	$R_{6/7}$ $R_{9/10}$ $R_{12/13}$		30		k $\Omega$	
AF-output resistance	$R_{8, 11, 14}$		100		$\Omega$	
Residual IF-voltage	$V_{IF8, 11, 14}$			5	mV	
Hum suppression (without deemphasis)	$a_H$		25		dB	$V_S = 5$ V; $V_H = 250$ mVpp; $f_H = 50$ Hz

## Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
<b>I<sup>2</sup>C Bus (SCL, SDA)</b>						
Edges SCL, SDA						
Rise time	$t_R$			1	$\mu\text{s}$	
Fall time	$t_F$			300	ns	
Shift clock SCL						
Frequency	$f_{\text{SCL}}$	0		100	kHz	
H-pulse width	$t_H$	4			$\mu\text{s}$	
L-pulse width	$t_L$	4			$\mu\text{s}$	
Start						
Setup time	$t_{\text{SUSTA}}$	4			$\mu\text{s}$	
Hold time	$t_{\text{HDSTA}}$	4			$\mu\text{s}$	
Stop						
Setup time	$t_{\text{SUSTO}}$	4			$\mu\text{s}$	
Bus free	$t_{\text{BUF}}$	4			$\mu\text{s}$	
Data change						
Setup time	$t_{\text{SUDAT}}$	1			$\mu\text{s}$	
Hold time	$t_{\text{HDDAT}}$	1			$\mu\text{s}$	
Inputs SCL, SDA						
Input voltage	$V_{\text{IH}}$ $V_{\text{IL}}$	2.4		5.5 1	V V	
Input current	$I_{\text{IH}}$ $I_{\text{IL}}$			10 10	$\mu\text{A}$ $\mu\text{A}$	
Output SDA (open collector)						
Output voltage	$V_{\text{QH}}$ $V_{\text{QL}}$	4.5		5.5 0.4	V V	$R_L = 2.5 \text{ k}\Omega$ $I_{\text{QL}} = 3 \text{ mA}$
Address byte 1 = L	$V_{5L}$	0		1	V	
Address byte 2 = H or open	$V_{5H}$	2.4		5.5	V	

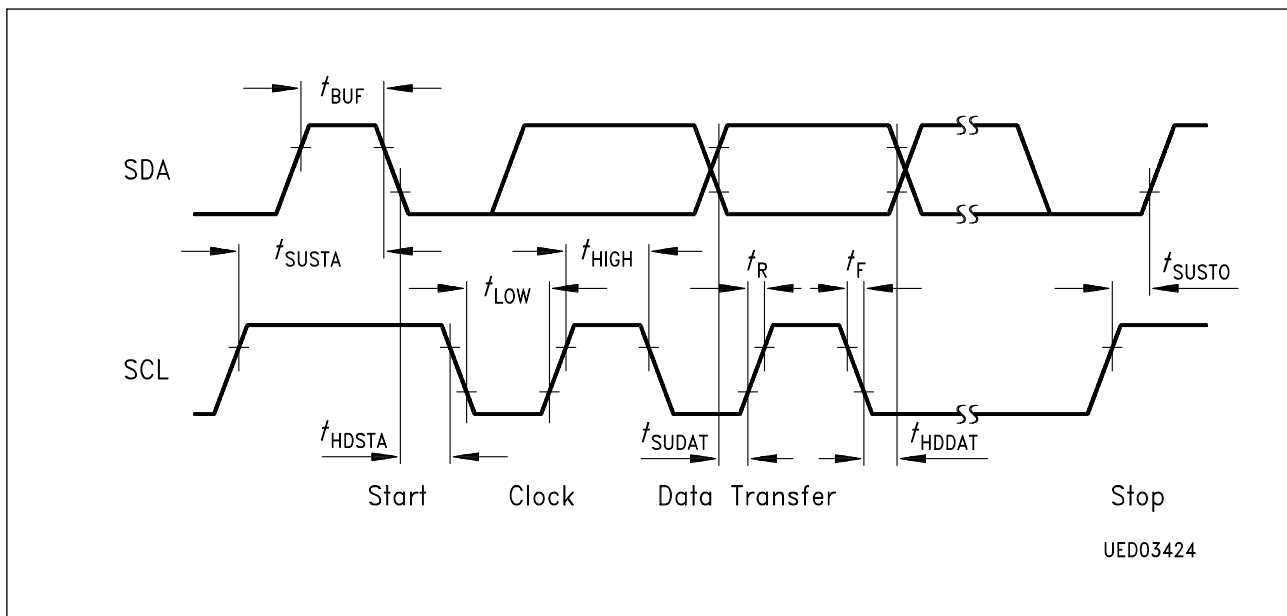


Test Circuit



Application Circuit





I<sup>2</sup>C Bus Timing Diagram

$t_{SUSTA}$	Setup time (start)
$t_{HDSTA}$	Hold time (start)
$t_H$	H-pulse width (clock)
$t_L$	L-pulse width (clock)
$t_{SUDAT}$	Setup time (data change)
$t_{HDDAT}$	Hold time (data change)
$t_{SUSTO}$	Setup time (stop)
$t_{BUF}$	Bus free time
$t_F$	Fall time
$t_R$	Rise time

All times referred to  $V_{IH}$  and  $V_{IL}$  values